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the energy barrier between said non-single crystal semiconductor layer and said film being lower than the energy barrier between said III-V compound semiconductor body and said film.

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10. An ohmic electrode obtained by annealing a multi-layered structure for fabricating an ohmic electrode, comprising a non-single crystal semiconductor layer comprising In and a film including at least a metal nitride film which are sequentially stacked on a III-V compound semiconductor body.

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14. The ohmic electrode according to claim 10 obtained by annealing said multi-layered structure for fabricating an ohmic electrode in which said film comprises a metal film and [a] wherein the metal nitride film is provided on said metal film.

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16. The ohmic electrode according to claim 15 obtained by annealing said multi-layered structure for fabricating an ohmic electrode in which a further metal film for wiring is provided on said refractory metal film.

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19. An ohmic electrode provided on a III-V compound semiconductor body obtained by annealing a multi-layered structure for fabricating an ohmic electrode, comprising a non-single crystal semiconductor layer comprised of In and a film including at least a metal nitride film,

the energy barrier between said non-single crystal semiconductor layer and said film being lower than the energy barrier between said III-V compound semiconductor body and said film.

REMARKS

Applicants have amended the claims to overcome the rejections of the Examiner under 35 U.S.C. §112, second paragraph. Applicants submit that the amended claims comport with the requirements of §112 and accordingly request that the Examiner withdraw these rejections.

Applicants respectfully request reconsideration of the prior art rejections under 35 U.S.C. §103. Applicants submit that the references cited by the